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Description

METHOD FOR SELECTIVE ELECTROPLATING OF SEMICONDUCTOR DEVICE I/O PADS USING A TITANIUM-TUNGSTEN SEED LAYER

BACKGROUND OF INVENTION

[0001] The present invention relates generally to semiconductor device processing and, more particularly, to a method for selective electroplating of semiconductor device I/O pads using a titanium-tungsten (TiW) seed layer.

[0002] In the manufacture of semiconductor devices, a selective plating process has been developed in order to plate copper, nickel, gold and other conductive metals on coils, vias, pads and other interconnect structures. In this selective plating process, electrical current is conducted through a layer of refractory metal (e.g., tantalum/tantalum nitride (Ta/TaN)) to plate metal on lines or pads using copper seed. The plating conditions are specifically de-

signed so as to enable deposition on pre-patterned copper pads only, not on the Ta/TaN seed. Because there is no photoresist used during the plating process, any over-plating otherwise caused by delamination of photoresist and bath contamination due to photoresist leaching is eliminated. Moreover, through the use of nickel/gold plating, the sidewalls of the copper seed are completely covered with the nickel/gold, thereby providing excellent corrosion resistance with this "self-encapsulated" metallurgy and eliminating the need for an extra passivation layer.

[0003] In addition, the use of selective copper plating can afford the opportunity for reduced chemical-mechanical polishing (CMP) time since less "extraneous" copper is formed from the plating. Pads with nickel and gold may be used either for wirebonding with thicker gold or for lead-free solder paste screening as capture pads with a flash of gold. The gold on the capture pad is demonstrated to exhibit very low contact resistance, which is ideal for electrical testing before C4 bumping. Furthermore, the electroplated nickel and gold as terminal metals has demonstrated promising results in stress tests. More specifically, it has opened up tremendous opportunities for pitch re-

duction, as well as a more protective surface for low-k dielectrics underneath at a lower test force and better reliability performance. After the completion of the metal plating, the Ta/TaN seed layer is removed by either a reactive ion etch process or a CMP process.

[0004] However, conventional selective plating processes are not without their own disadvantages. First, there is a thickness uniformity issue associated with using a Ta/TaN seed layer. A Ta/TaN seed layer at 800 Angstroms (Å) is considered very resistive. In the case of copper plating, the edge areas can be plated to a thickness about twice that of the center areas, which is not acceptable for applications where copper uniformity is critical. Second, the presence of surface topography (e.g., corners or other defects) in the seed layer can dramatically increase local plating currents. In certain cases, these local currents can be too high and thus start to plate metal on the Ta/TaN seed. In turn, the over-plated metal nodules can short the electrical features of the device. Accordingly, the applied plating current density is kept fairly low, which results in longer plating times, as well as possibly changing the film microstructure and properties.

[0005] Still another disadvantage of conventional selective plating

results from the Ta/TaN removal process (i.e., reactive ion etching). A reactive ion etch (RIE) process has the effect of removing some gold from the surface. Although the loss of gold can be compensated for, the redeposition of gold on the manufacturing tool presents a manufacturing concern. On the other hand, a resulting thinner gold layer can lead to wire bond failures. CMP is also not a desirable method for Ta/TaN seed removal, due to the topographic features of the structure. A third possibility is a wet chemical etch to remove the Ta/TaN seed, however the etchant materials are difficult to handle from a manufacturing standpoint.

[0006] Accordingly, it would be desirable to implement a selective plating process that also allows for higher conductivity and tool throughput, and without the disadvantages as mentioned above.

SUMMARY OF INVENTION

[0007] The foregoing discussed drawbacks and deficiencies of the prior art are overcome or alleviated by a method for selective electroplating of a semiconductor input/output (I/O) pad. In an exemplary embodiment, the method includes forming a titanium-tungsten (TiW) layer over a passivation layer on a semiconductor substrate, the TiW

layer further extending into an opening formed in the passivation layer for exposing the I/O pad, such that the TiW layer covers sidewalls of the opening and a top surface of the I/O pad. A seed layer is formed over the TiW layer, and portions of the seed layer are selectively removed such that remaining seed layer material corresponds to a desired location of interconnect metallurgy for the I/O pad. At least one metal layer is electroplated over the remaining seed layer material, using the TiW layer as a conductive electroplating medium.

[0008] In another aspect, a semiconductor input/output (I/O) pad structure includes a titanium-tungsten (TiW) layer formed into an opening formed in a passivation layer on a semiconductor substrate, the opening created for exposing an I/O pad, such that said TiW layer further covers sidewalls of the opening and a top surface of the I/O pad. A seed layer is formed over a portion of the TiW layer and corresponding to a desired location of interconnect metallurgy for the I/O pad. At least one metal layer is electroplated over the seed layer, wherein the TiW layer serves as a conductive electroplating medium.

Brief Description of Drawings

[0009] Referring to the exemplary drawings wherein like ele-

ments are numbered alike in the several Figures:

[0010] Figures 1 through 8 illustrate various processing steps of a method for selective electroplating of semiconductor device I/O pads using a titanium-tungsten (TiW) seed layer, in accordance with an embodiment of the invention.

DETAILED DESCRIPTION

[0011] Disclosed herein is a method and structure for selective electroplating of semiconductor device I/O pads using a titanium-tungsten (TiW) seed layer. The TiW seed layer provides improved plating uniformity and significantly increased conductivity as compared to a Ta/TaN conducting seed layer. In addition, the use of TiW as described below addresses sputtering concerns of Ta/TaN on polyimides, as well as gold loss during reactive ion etching.

[0012] Referring initially to Figure 1, there is shown a cross-sectional view of an exemplary terminal metal (TD) aluminum bond pad structure 100, suitable for use in accordance with an embodiment of the invention. The structure 100 features an aluminum bond pad 102 formed at an uppermost metallization level of a semiconductor substrate 104, and which serves to provide an external connection to the active devices (not shown) formed in the substrate through various levels of interconnect structures

there between, including an aluminum filled via 106. Surrounding the aluminum pad 102 and via 106 are alternating layers of dielectric 108 (e.g., SiO_2 or low-k material) and pad nitride 110 (e.g., Si_3N_4), as will be recognized by those skilled in the art. In addition, a passivation layer, such as a photosensitive polyimide (PSPI) layer 112 is formed over the topmost pad nitride layer 110.

[0013] In order to provide access for a suitable external connection, a via or opening 114 is formed over the top surface of the aluminum pad 102. As shown in Figure 2, a layer 116 of titanium-tungsten (TiW) is deposited over the entire structure (including the sidewalls of the via 114 and the top of the aluminum pad 102), followed by a layer 118 of copper/chrome-copper (Cu/CrCu) seed. Although Figure 2 depicts layer 118 as a single layer, it should be understood that the Cu/CrCu seed may be a multilayer. As stated earlier, the entire layer 118 of Cu/CrCu was heretofore used as a seed layer, with all regions outside of the via area being protected with photoresist during the plating step, such that the plating metal would only be formed on the exposed portions of the Cu/CrCu. In the present method, however, the Cu/CrCu is first removed in all locations except for the via 114 region where the inter-

connect metallurgy is to be formed.

[0014] Accordingly, Figure 3 illustrates the patterning of the via 114 regions (at which the Cu/CrCu 118 layer is to remain) with photoresist 120. Thereafter, the unmasked portions of the Cu/CrCu layer 118 are electroetched away, stopping on the TiW layer 116 as shown in Figure 4. Additional information regarding electroetch processes and techniques may be found, for example, in U.S. Patent 5,486,282 to Datta et al. and in U.S. Patent 5,536,388 to Dinan et al., the contents of which are incorporated herein in their entirety. Then, the remaining photoresist 120 is stripped away (Figure 5), and the electroplating of a nickel layer 122 and gold layer 124 is implemented as shown in Figure 6. Because the Cu/CrCu layer 118 is only present in the via 114 regions, it acts as a seed layer for the electroplating. Furthermore, the continuous TiW layer 116 acts as the current carrying layer for providing the electroplating conductivity, but none of the electroplated material (Ni, Au) is formed thereupon. This may be accomplished by balancing the applied potential so that the nickel will nucleate on the Cu/CrCu seed layer 118, but not on the TiW layer 116.

[0015] It will also be noted from Figure 6 that, in contrast to con-

ventional electroplating with a protected Cu/CrCu seed layer, the sidewalls of the remaining Cu/CrCu material in the via 114 regions are encapsulated by the electroplated material, since there is no photoresist present during the actual electroplating step. This results in improved corrosion resistance of the Cu/CrCu material. Once the interconnect metallurgy is formed, the remaining portions of TiW layer 116 not covered by the interconnect metallurgy are removed by a wet etch. Finally, as shown in Figure 8, the bond pad structure 100 is ready for a subsequent processing step, such as the addition of a lead-free solder paste 126 in preparation for C4 ball attachment, for example. Alternatively, a wirebond attachment could also be used in conjunction with the bond pad structure 100.

[0016] The use of TiW as a conductive electroplating seed material offers several advantages with respect to a Ta/TaN layer. First, the seed thickness of the TiW can be applied up to about 6000Å, providing good coverage over the surface topography and also lowering the sheet resistance. For example, such a thickness of TiW is estimated to be about 10 times as conductive than a Ta liner formed at about 700Å, leading to better plating uniformity. In addition, TiW has a higher overpotential for nickel and gold

plating. As such, the amount of electrical current that may be passed through a TiW layer can be about three times greater than for a Ta/TaN layer, and without the formation of nodules on the layer. This results in improved tool throughput by about 300%. Also, because TiW is an established material for C4 ball limiting metallurgy (BLM), the TiW etch process may be easily implemented with a hydrogen peroxide chemistry and end-point detection control. An exemplary TiW etch process is described in U.S. Patent 6,293,457 to Srivastava, et al., the contents of which are incorporated herein in their entirety. Moreover, the thickness of the gold layer is undisturbed during the TiW etch process.

[0017] While the invention has been described with reference to a preferred embodiment or embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best

mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims.